



### Designing A Wide Input Range DCM Flyback Converter **Using the Si9108**

#### **FEATURES**

- Wide 10-V to 100-V Input Voltage Range
- Enables Designs With Efficiency Above 80%
- ±12-V Outputs At 125 mA
- Total 3-W Continuous Power
- Discontinuous Conduction Mode Flyback dc-to-dc Converter
- 500-V Input/Output Isolation Minimum
- No Optocoupler Feedback Needed
- Low Component Count, Low-cost Design
- Complete Solution Occupies < 2 In<sup>2</sup> Of Board Space In A Single-Sided FR4 Board
- Maximum Component Height Is  $< \frac{1}{4}$  Inch.

#### **INTRODUCTION**

The Si9108 is a highly integrated, high-efficiency current-mode regulator designed for telecom dc-to-dc converters. Its wide operating duty cycle of up to 99.9% is suitable for many power conversion applications, especially those with a wide operating input voltage range. This application note is intended to guide the user to design a very wide input voltage range, discontinuous conduction mode (DCM) flyback converter.

Why use a flyback converter? Because the flyback design combines simplicity, a low parts count, and affordability for low-power applications that require input/output isolation.

Why use discontinuous conduction mode? Here are some of the advantages:

maximizes energy storage in the magnetic component (a smaller core is needed for a given output power)

- eliminates the output rectifying diode reverse recovery problem, hence there is no current shoot through in the main input power switching device
- higher efficiency, especially at high input voltage
- no right half plane zero in the control loop, simplifying feedback compensation design, allowing a very stable and wide-bandwidth feedback loop.

A DCM Flyback Design Has Some Limitations:

- the peak primary current and output rectifying diode current are large, although this is not a major concern for low-power applications
- duty cycle varies with both the input voltage and output load, thus wide duty cycle operation is usually required.

The design of the Si9108 regulator helps to overcome this limitation. Figure 1 illustrates a simplified flyback converter designed with the Si9108 regulator.

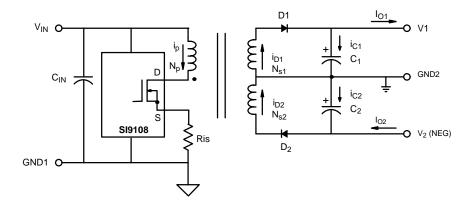


FIGURE 1. Simplified Flyback Converter Using Si9108 Regulator

#### **Discontinuous Flyback Converter Fundamentals**

Figure 2 shows typical current waveforms of a DCM flyback converter in operation.

To simplify circuit analysis, we can convert the flyback circuit to a basic buck-boost converter configuration. The conversion can be done in two steps:

Step one: converting all outputs into a single output. Let  $V_O = V_{O1}$ , and  $P_O = V_{O1} \times I_{O1} + V_{O2} \times I_{O2} \rightarrow I_O = P_O/V_O$ 

Step two: reflecting the input voltage to the output side. $V_S =$ V<sub>i</sub>(Ns/Np)

Where Ns is the secondary number of turns and Np is the primary number of turns. Figure 3 shows the simplified buck-boost converter.

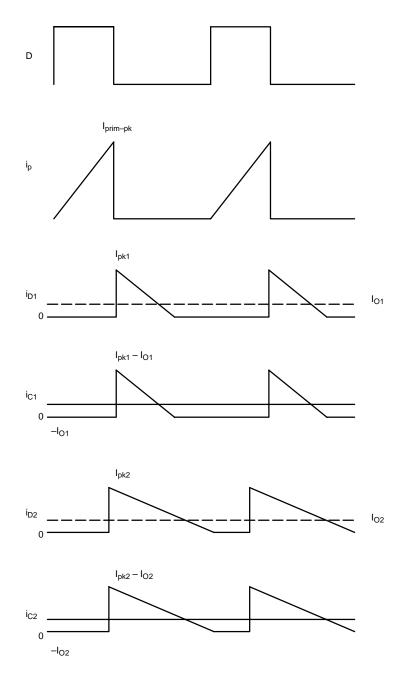
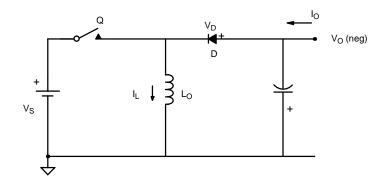


FIGURE 2. Typical Current Waveforms of DCM Flyback

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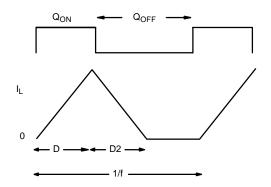


FIGURE 3. Basic Buck-Boost Converter

#### **DCM Buck-Boost Converter Analysis**

The inductor charging time interval is designated as t1. When the power switch Q is on, V<sub>S</sub> is applied across the output inductor, Lo. The current in the inductor starts to ramp up from zero linearly, following the equation V = L(di/dt). By the end of this interval, when Q turns off, the inductor will have a peak current of

$$lpk = \frac{V_S D}{Lof}$$
 (1)

where D is the duty cycle and f is the switching frequency.

lpk indicates that a certain amount of energy has been stored in the inductor. The inductor discharging time interval is designated as t2. After Q turns off, the current in Lo forces diode D to conduct. Lo sees the output voltage plus the diode forward voltage drop across its terminal, but in the reverse direction. During this time, the inductor current decreases and the energy in Lo is discharged to the output capacitor and load. In DCM operation, all of the energy in Lo will discharge completely during this time interval. An equation similar to t1 results:

$$lpk = \frac{V_O D2}{Lof}$$
 (2)

where D2 is the discharging cycle and Vo is the lump sum of the output voltage plus the rectifying diode forward voltage drop.

After this time interval, all of the energy stored in Lo has been discharged to the output capacitor and load. The current in Lo has decreased to zero. The inductor current will remain at zero until the next cycle start.

For every switching cycle, a package of energy is transferred to the output via Lo. The power associated with this energy transfer is:

$$P = \frac{1}{2} \text{ Lolp}\kappa^2$$
 or 
$$\text{lp}\kappa = \sqrt{\frac{2P}{\text{Lof}}}$$
 (3)

Combining the above equations and solving for D and D2:

$$D = \frac{1}{Vs} \sqrt{2PLof}$$
 (4)

$$D2 = \frac{1}{V_0} \sqrt{2PLof}$$
 (5)

Equation (4) shows the duty cycle as a function of the output power and input voltage, while equation (5) shows that D2 is solely a function of the output power. The maximum duty cycle, DM, occurs at maximum output power, PM, and minimum input voltage, Vsm. Maximum D2 occurs at maximum output power.



To maintain DCM operation, the inductor current must discharge completely before the next cycle start. In other words, D + D2 must be equal or less than 1 under all conditions:

$$DM + D2M \le 1 \tag{6}$$

where DM is the maximum duty cycle and D2M is the maximum discharging cycle. Substituting (4) and (5) into the above equation and solving for Lo, we have:

$$Lo \leq \frac{1}{2PMf\left(\frac{1}{Vsm} + \frac{1}{Vo}\right)^{2}}$$

$$Locrit = \frac{1}{2PMf\left(\frac{1}{Vsm} + \frac{1}{Vo}\right)^{2}}$$
(7)

where PM is the maximum output power and Vsm is the minimum input voltage.

Equation (7) imposes a maximum value for the output inductor, Locrit, to maintain discontinuous conduction mode while delivering the maximum output power at minimum input voltage for a buck-boost converter. It is best to choose a Lo value close to Locrit to maintain DCM while keeping the inductor peak current as low as possible.

#### **Back to The Flyback Converter**

In a flyback converter, the flyback transformer presents designers with another choice, the secondary-to-primary turns ratio Ns/Np. The following equation was derived to assist the calculation of the turns ratio.

$$\frac{Ns}{Np} = \frac{Vo}{Vim} \frac{(1 - DM)}{DM}$$
 (8)

where Vim is the minimum input voltage. Ns/Np determines a maximum duty cycle or in other words, allows designers to choose a practical maximum duty cycle at the lowest operating input voltage and then calculate the required transformer turns ratio. It will be shown later that choosing DM is very important to optimize the converter design.

The following equations can be used to calculate the critical output inductance once the maximum duty cycle is chosen.

$$Lo \le \frac{Vo^2 (1 - DM)^2}{2PMf}$$
Or
$$Locrit = \frac{Vo^2 (1 - DM)^2}{2PMf}$$
(9)

Again, choose Lo = Locrit, since

$$Ip_{K} = \sqrt{\frac{2P}{Lof}}$$
 (10)

Combining (9) and (10), we can now express the inductor peak current in terms of the maximum duty cycle chosen:

$$Ip\kappa = \frac{2PM}{Vo(1 - DM)} \tag{11}$$

As DM increases, the required inductance decreases, while the inductor peak current increases. Since the energy storage in the inductor is proportional to Llpk<sup>2</sup> while the inductor core size is proportional only to Llpk, doubling lpk will reduce the required inductance to  $^{1}/_{4}$ . and reduce the required core size to  $^{1}/_{2}$ . It is a good design practice to make D as large as possible. This minimizes inductance while keeping the peak current to a manageable value.

#### **Primary Side Calculations**

The primary inductance and peak current can be calculated by reflecting the output inductance and its peak current to the primary side via the flyback transformer turns ratio:

$$Lp = \left(\frac{Np}{Ns}\right)^{2} Lo$$

$$Iip\kappa = \frac{Ns}{Np} \sqrt{\frac{2P}{Lof}}$$
(12)

where Lp is the primary inductance required and lipk is the primary peak current as a function of total output power. Since  $V_S = Vi(Ns/Np)$  and from (4):

$$D = \frac{Np}{NsVi} \sqrt{2PLof}$$
 (13)

As expected, the duty cycle D is a function of the input voltage, Vi, and the output power, P.

From (12) and (13), several equations can be derived to support design calculation:

liave = 
$$\frac{1}{2} \text{ lip}_K D = \frac{P}{vi}$$
  
lirms = lip $K \sqrt{\frac{D}{3}}$   
lcirms = liave  $\sqrt{\frac{D^2}{6} + \left(\frac{2-D}{6D}\right)^3 + (1-D)}$  (14)  
 $\Delta V \text{ci} = \frac{1}{4} \frac{\text{liave}}{\text{Cif}} (2-D)^2$ 

#### where

liave is the primary average current lirms is the primary rms current lcirms is the input capacitor rms current  $\Delta V ci$  is the input voltage ripple, excluding ESR effect Ci is the input bypass capacitor

#### **Output Calculations**

Any output can be calculated referencing to the main output using the following equations:

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$$Nsx = \frac{Vx}{Vo} Ns$$

$$Lx = \left(\frac{Nx}{Ns}\right)^{2} Lo$$

$$Dx = \frac{1}{Vx} \sqrt{2PxLx}f$$

$$Ixpk = \sqrt{\frac{2Px}{Lx}f}$$

$$Ixrms = Ixpk \sqrt{\frac{Dx}{3}}$$

$$Icxrms = lox \sqrt{\frac{DX^{2}}{6} + \left(\frac{2 - Dx}{6Dx}\right)^{3} + (1 - Dx)}$$

$$\Delta Vcx = \frac{1}{4} \frac{lox}{Cxf} (2 - Dx)^{2}$$



X denotes the particular output of interest Vx is the output voltage plus the rectifier forward voltage drop Nsx is the winding number of turns Lx is the winding inductance Dx is the discharge duty cycle Px is the output power lxpk is the inductor, Lx, peak current lxrms is the inductor rms current lcxrms is the output capacitor rms current lox is the output average load current ΔVcx is the output voltage ripple, excluding capacitor ESR and ESL effects

#### **Design Example**

Cx is the output capacitor

This design example is based on the following specifications:

Input voltage range: Vi from 10 V to 100 V

Output voltages: +12 V and -12 V at 125 mA each

Total output power is 3 W

Output power is reduced to 1 W for

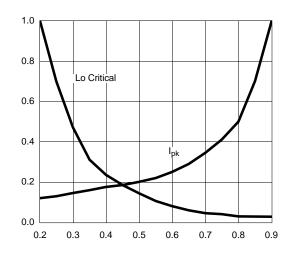
input voltage <24 V

Switching frequency: 100 kHz

#### Calculation

Let us assume an efficiency of 75% and lump sum inductor tolerance of 20%, plus 20% for power limit headroom. In this case, the total power processed by the flyback converter is:

$$P = 3 W \frac{1}{0.75} (1 + 40\%) = 5.6 W$$
 (16)



Maximum Duty Cycle Chosen

**FIGURE 4.** Normalized Lo Critical and  $I_{pk}$  vs. Maximum Duty Cycle

Figure 4 above shows the normalized critical output inductance and its peak current with respect to a maximum duty cycle varying from 20% to 90%. From the graph, we can see that Lo decreases significantly for DM >40% and its peak current decreases significantly for DM < 80%. This means that it is desirable to choose DM anywhere in the 40% to 80% region.

Choose DM = 55% at full load and 24 V. Use Vo = 12 V as reference output plus 0.6 V for the rectifier forward voltage drop. We can now determine the required nominal output inductance. Notice that the inductor tolerance has already been accounted for in the power calculation. The 55% DM was chosen at a 24-V input so that at a 10-V input and with 1-W output power, the duty cycle will be around 80%—still an acceptable level.

$$Lo = \frac{Vo^{2} (1 - DM)^{2}}{2PMf} = \frac{12.6^{2} (1 - 0.55)^{2}}{2x5.6x100\kappa} = 28.7\mu H$$
(17)

Next, calculate the transformer turns ratio:

$$\frac{Ns}{Np} = \frac{V_0}{Vim} \frac{(1 - DM)}{DM} = \frac{12.6}{24} \frac{(1 - 0.55)}{0.55} = 0.4295$$
 (18)

Choose Ns = 40T and Np = 95T. Transformer specification details will be covered later.

From this point on, the calculation of the rest of the circuit parameters is relatively straightforward:

Transformer primary inductance:

$$Lp = \left(\frac{Np}{Ns}\right)^2 Lo = \left(\frac{95}{40}\right)^2 28.7 \mu H = 162 \mu H \tag{19}$$

Duty cycle, primary maximum peak and rms currents at a 24-V input voltage

$$\begin{split} \text{D} &= \frac{\text{Np}}{\text{NsVi}} \, \sqrt{2 \text{PLo} f} \, = \, \frac{95}{40 \text{x} 24} \, \sqrt{2 \text{x} 5.6 \text{x} 28.7 \mu \text{x} 100 \kappa} \, = \, 0.56 \\ \text{lip} &\kappa &= \frac{\text{Ns}}{\text{Np}} \, \sqrt{\frac{2 \text{P}}{\text{Lo} f}} \, = \, \frac{40}{95} \, \sqrt{\frac{2 \text{x} 5.6}{28.7 \mu 100 \kappa}} \, = \, 0.832 \text{Apk} \\ \text{lirms} &= \text{lip} &\kappa \, \sqrt{\frac{D}{3}} \, = \, 0.832 \, \sqrt{\frac{0.56}{3}} \, = \, 0.36 \text{Arms} \end{split}$$

Primary sense resistor, Ris, calculation:

$$Ris = \frac{0.8V}{lip_K} = \frac{0.8}{0.832} = 0.96 \text{ Ohm}$$
 (21)

where 0.8 V is the Si9108 current limit minimum threshold voltage. A 1- $\Omega$  sense resistor is used for this design.

#### **Output Calculation**

Since the +12 V and -12 V are identical, only one set of calculations is needed. The following is the calculation for a 12-V output. Since 12 V was used as the reference output voltage, its secondary winding number of turns and inductance is the same as Ns and Lo calculated earlier.

12-V output maximum power,

$$Px = Vxlox = 12x125 m = 1.5 W$$
 (22)

12-V secondary number of turns,

$$Nsx = 40T (23)$$

12-V secondary winding inductance,

$$Lx = 28.7 \,\mu\text{H}$$
 (24)

12-V secondary maximum discharging duty cycle,

$$Dx = \frac{1}{Vx} \sqrt{2PxLx}f = \frac{1}{12.6} \sqrt{2x1.5x28.7\mu100\kappa} = 0.23$$
 (25)

12-V secondary winding maximum peak and rms current,

$$\begin{aligned} \text{lxpk} &= \sqrt{\frac{2\text{Px}}{\text{Lx}f}} = \sqrt{\frac{2\text{x}1.5}{28.7\,\mu}} = 1.02\,\text{Apk} \\ \text{lxrms} &= \text{lxpk}\,\,\sqrt{\frac{\text{Dx}}{3}} = 1.02\,\,\sqrt{\frac{0.23}{3}} = 0.28\,\text{Arms} \end{aligned} \tag{26}$$

12-V output filter capacitor maximum ripple current and maximum output ripple voltage, using 10-μF low ESR ceramic capacitor for output filtering.

lcxrms = lox 
$$\sqrt{\frac{Dx^2}{6} + \left(\frac{2 - Dx}{6Dx}\right)^3 + (1 - DX)} =$$
  
125mA  $\sqrt{\frac{0.23^2}{6} + \left(\frac{2 - 0.28}{6x0.28}\right)^3 + (1 - 0.28)} = 168 \text{ mArms}$   
 $\Delta Vcx = \frac{1}{4} \frac{lox}{Cxf} (2 - Dx)^2$   
 $= \frac{1}{4} \frac{125 \text{ m}}{10 \text{ u}} \frac{100 \text{ k}}{100 \text{ k}} (2 - 0.28)^2 = 92.5 \text{ mVp_p}$ 

#### Transformer Specifications

The following parameters are needed to specify the DCM flyback transformer:

- Primary inductance, Lp = 162 μH ±20%
- Secondary/primary turns ratio, Ns/Np = 0.43 ± 0.01
- Other winding turns ratio, referenced to the main output turns ratio, if applicable
- All winding maximum rms currents, lirms = 0.36 Arms, Ixrms = 0.28 Arms, etc.
- The converter switching frequency, 100 kHz

An EFD10 core is recommended for this application, with 3F3 core material used for low core loss operation. The primary number of turns is 95T which gives a maximum flux density of 1000 Gauss (0.1 Testla). The secondary number of turns for both the +12-V and -12-V outputs is 40T. A 34T auxiliary winding is used to power Vcc and for feedback regulation. The Vcc feedback voltage is designed at 10 V. The Vishav Dale part number for this transformer is LPE-4658-A409.

#### **Experimental Results and Other Design Considerations**

Figures 5 through 7 show the complete schematic of the design, together with its bill of materials and pcb layout artworks.

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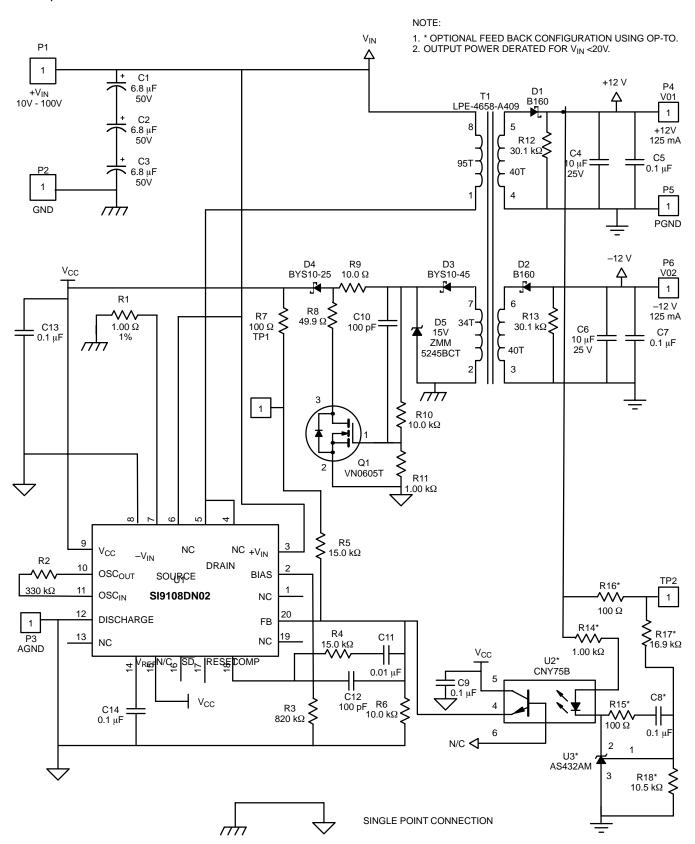


FIGURE 5. Complete Schematic



| TABLE 1. BILL OF MATERIAL |     |                              |                |                         |              |                  |                        |  |  |  |  |  |
|---------------------------|-----|------------------------------|----------------|-------------------------|--------------|------------------|------------------------|--|--|--|--|--|
| tem                       | Qty | Designator                   | Part Type      | Description             | Footprint    | Vendor Part#     | Manufacturer           |  |  |  |  |  |
| 1                         | 1   | R1                           | 1.00           | RES,1%, 1/8W            | 0805         | CRCW08051R00FRT1 | VISHAY DALE            |  |  |  |  |  |
| 2                         | 1   | R2                           | 330K           | RES,1%, 1/8W            | 0805         | CRCW08053303FRT1 | VISHAY DALE            |  |  |  |  |  |
| 3                         | 1   | R3                           | 820K           | RES,1%, 1/8W            | 0805         | CRCW08058203FRT1 | VISHAY DALE            |  |  |  |  |  |
| 4                         | 2   | R4, R5                       | 15.0K          | RES,1%, 1/8W            | 0805         | CRCW08051502FRT1 | VISHAY DALE            |  |  |  |  |  |
| 5                         | 2   | R6, R10                      | 10.0K          | RES,1%, 1/8W            | 0805         | CRCW08051002FRT1 | VISHAY DALE            |  |  |  |  |  |
| 6                         | 1   | R7, R15*, R16*               | 100            | RES,1%, 1/8W            | 0805         | CRCW08051000FRT1 | VISHAY DALE            |  |  |  |  |  |
| 7                         | 1   | R8                           | 49.9           | RES,1%, 1/8W            | 0805         | CRCW080549R9FRT1 | VISHAY DALE            |  |  |  |  |  |
| 8                         | 1   | R9                           | 10.0           | RES,1%, 1/8W            | 0805         | CRCW080510R0FRT1 | VISHAY DALE            |  |  |  |  |  |
| 9                         | 1   | R11, R14*                    | 1.00K          | RES,1%, 1/8W            | 0805         | CRCW08051001FRT1 | VISHAY DALE            |  |  |  |  |  |
| 10                        | 2   | R12, R13                     | 30.1K          | RES,1%, 1/8W            | 0805         | CRCW08053012FRT1 | VISHAY DALE            |  |  |  |  |  |
| 11                        | 0   | R17*                         | 16.9K          | RES,1%, 1/8W            | 0805         | CRCW08051692FRT1 | VISHAY DALE            |  |  |  |  |  |
| 12                        | 1   | R18                          | 10.5K          | RES,1%, 1/8W            | 0805         | CRCW08051052FRT1 | VISHAY DALE            |  |  |  |  |  |
|                           | l . |                              |                |                         |              |                  |                        |  |  |  |  |  |
| 13                        | 3   | C1, C2, C3                   | 6.8uF          | CAP, TAN, 50V, 20%      | 595D_C       | 595D685X0050C2T  | VISHAY SPRAGUE         |  |  |  |  |  |
| 14                        | 2   | C4, C6                       | 10uF           | CAP, CER, X5R, 25V, 10% | 1812         | GRM43-2X5R106K25 | MURATA                 |  |  |  |  |  |
| 15                        | 5   | C5, C7, C8*,<br>C9, C13, C14 | 0.1uF          | CAP, CER, Z5U, 50V, 10% | 0805         | VJ0805Y104KXAAT  | VISHAY VITRAMON        |  |  |  |  |  |
| 16                        | 2   | C10, C12                     | 100pF          | CAP, CER, X7R, 50V, 10% | 0805         | VJ0805Y101KXAAT  | VISHAY VITRAMON        |  |  |  |  |  |
| 17                        | 1   | C11                          | 0.01uF         | CAP, CER, X7R, 50V, 10% | 0805         | VJ0805Y103KXAAT  | VISHAY VITRAMON        |  |  |  |  |  |
|                           |     |                              |                |                         |              |                  |                        |  |  |  |  |  |
| 18                        | 2   | D1, D2                       | B160           | SCHOTTKY DIODE, 35V     | SMA          | B160             | LITEON                 |  |  |  |  |  |
| 19                        | 1   | D3                           | BYS10-45       | SCHOTTKY DIODE, 45V     | BYS10        | BYS10-45         | VISHAY TELEFUNKEN      |  |  |  |  |  |
| 20                        | 1   | D4                           | BYS10-25       | SCHOTTKY DIODE, 25V     | BYS10        | BYS10-25         | VISHAY TELEFUNKEN      |  |  |  |  |  |
| 21                        | 1   | D5                           | ZMM5245BCT     | ZENER DIODE, 15V        | MiniMELF     | ZMM5245BCT       | LITEON                 |  |  |  |  |  |
| 22                        | 1   | T1                           | LPE-4658-A409  | TRANSFORMER             | XFMR_LPE4658 | LPE-4658-A409    | VISHAY DALE            |  |  |  |  |  |
|                           |     | l                            |                | <u> </u>                | <u> </u>     |                  | I                      |  |  |  |  |  |
| 23                        | 1   | U1                           | SI9108DN02     | POWER IC                | PLCC-20      | SI9108DN02       | VISHAY SILICONIX       |  |  |  |  |  |
| 24                        | 0   | U2*                          | CNY75B         | OPTOCOUPLER             | DIP6         | CNY75B           | VISHAY TELEFUNKEN      |  |  |  |  |  |
| 25                        | 0   | U3*                          | AS432AM        | ADJ SHUNT REGULATOR     | SOT-23       | AS432AM          | ALPHA<br>SEMICONDUCTOR |  |  |  |  |  |
| 26                        | 1   | 04                           | VNOCOET        | N CHANNEL MOSEET        | SOT 22       | VNIOCOET         | MISHAY SHI IOONIY      |  |  |  |  |  |
| 26                        | 1   | Q1                           | VN0605T        | N-CHANNEL MOSFET        | SOT-23       | VN0605T          | VISHAY SILICONIX       |  |  |  |  |  |
| 27                        | 8   | P1 TO P6, TP1,<br>TP2        | POWER, GND, TP | 1 PIN HEADER            | TP1          |                  | MULTI-SOURCE           |  |  |  |  |  |

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Note
\* Optional Component, not needed unless opto-feedback is required.



### **PCB LAYOUT—Si9108DB**

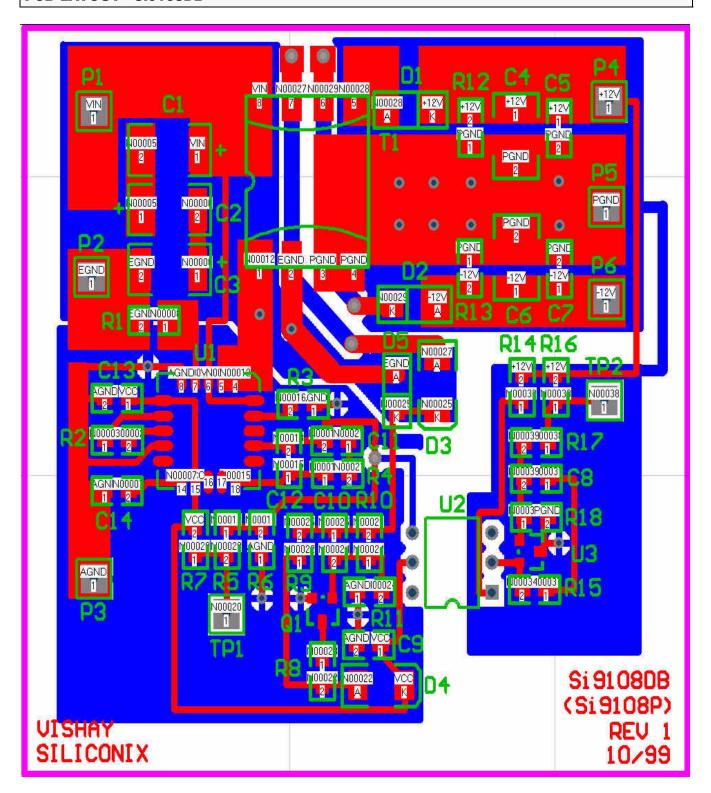


FIGURE 6. Layout Artwork



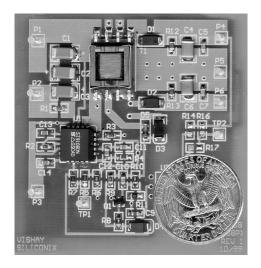


FIGURE 7. Picture of Demoboard

### **Optocoupler Feedback**

This converter design obtains output regulation through coupled windings between the V<sub>CC</sub> reference winding (T1 pin 7 to pin 2) and the output windings. As a result, optocoupler feedback is not required. A special technique was used to wind the transformer to ensure good coupling. U2, U3, R14 through R18, and C8 are optional components for the optocoupler feedback configuration and were not used on our test board. For applications that need tight output voltage regulation, optocoupler feedback circuitry should be used.

Leakage snubber: No matter how well the transformer is made, a certain amount of leakage inductance is unavoidable in each of the windings. The leakage inductance energy in the V<sub>CC</sub> reference winding imposes a positive offset on to the V<sub>CC</sub> regulation voltage level, thus lowering the voltage on other outputs. A leakage snubbing circuit is employed (Q1, R8, R9, R10, R11, C10, and D3) here to provide better output regulation. For applications with an optocoupler feedback configuration, the leakage snubbing circuit is not needed.

Preload: To reduce leakage inductance effects on the outputs, especially at light load conditions, pre-load resistors R12 and R13 are used. The larger the pre-load (smaller resistance), the better the voltage regulation at light loads, although this means a trade off of more power losses. For applications where the output current is maintained at a minimum of 10% of the full load current, these preload resistors are not needed.

Table 2 shows some typical efficiency and regulation measurements. Efficiency above 80% is typical for most operating conditions.

| V <sub>IN</sub> (V) | I <sub>IN</sub> (A)   | +12 V<br>(V) | I +12 V<br>(A) | –12 V<br>(V) | I –12 V<br>(A) | PO (W) | Efficiency<br>(%) |
|---------------------|-----------------------|--------------|----------------|--------------|----------------|--------|-------------------|
| 24.07               | 0.1500                | 11.85        | 0.1270         | 11.31        | 0.1256         | 2.93   | 81.0              |
| 23.94               | 0.0751                | 12.14        | 0.0627         | 11.56        | 0.0656         | 1.52   | 84.5              |
| 24.24               | 0.0240                | 12.33        | 0.0307         | 12.06        | 0.0107         | 0.51   | 87.3              |
| 23.82               | 0.0901                | 12.38        | 0.0300         | 11.16        | 0.1260         | 1.78   | 82.8              |
|                     | •                     |              |                |              |                |        | •                 |
| 99.56               | 0.0330                | 11.86        | 0.1269         | 11.32        | 0.1374         | 3.06   | 93.1              |
| 99.72               | 0.0061                | 12.34        | 0.0312         | 12.14        | 0.0159         | 0.58   | 94.4              |
|                     |                       |              |                |              |                |        |                   |
| 12.00               | 0.1437                | 12.17        | 0.0538         | 11.56        | 0.0580         | 1.32   | 76.8              |
| 12.07               | 0.0735                | 12.36        | 0.0261         | 11.70        | 0.0335         | 0.71   | 80.5              |
| 12.06               | 0.0190                | 12.68        | 0.0052         | 11.97        | 0.0061         | 0.14   | 60.8              |
|                     | V <sub>OUT(min)</sub> | 11.850       |                | 11.160       |                |        |                   |
|                     | V <sub>OUT(max)</sub> | 12.680       |                | 12.140       |                |        |                   |
|                     | V <sub>OUT(nom)</sub> | 12.265       |                | 11.650       |                |        |                   |
|                     | tol ±                 | 3.38%        |                | 4.21%        |                |        |                   |

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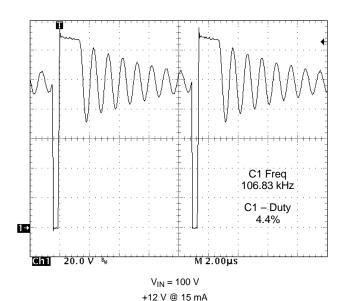
Figures 8, 9, and 10 show waveforms of the power switch drain-to-source voltage, the primary current, and the ouput voltage ripples. The minimum duty cycle occurs at light loads and high lines and is around 5% at a 100-V input and 30 mA at –12 V and 15 mA at +12 V. The worst-case maximum duty cycle is at full load and low line and is around 52% at a 24-V input and 125 mA on each of the outputs. The measured primary peak current is 600 mA, which corresponds to calculations using measurement data.

P = 2.92 W at 81% efficiency = 3.6 W

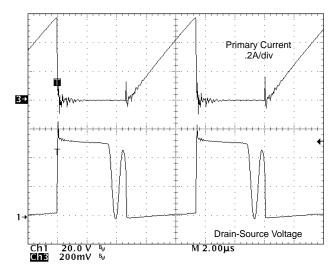
$$lip_{K} = \frac{Ns}{Np} \sqrt{\frac{2P}{Lof}} = \frac{40}{95} \sqrt{\frac{2x3.6}{28.7 \,\mu 106 \,\kappa}} = 648 \,\text{mA}$$
 (28)

#### CONCLUSION

A dual outputs, 3W, discontinuous conduction mode flyback converter was designed, built and tested. The converter features a very wide operating input voltage range with efficiency above 80%. Input output isolation is provided without the use of opto-coupler feedback. Total components occupy less than  $2 \, \text{in}^2$  of board space in a single sided FR4 board. The maximum component height is less than  $^{1}/_{4}$  of an inch.



-12 V @ 30 mA FIGURE 8. Drain-Source Voltage of Power Switch



 $V_{IN} = 24 \text{ V}$ ± 12 V @ 125 mA

FIGURE 9. Drain-Source Voltage and Primary Current

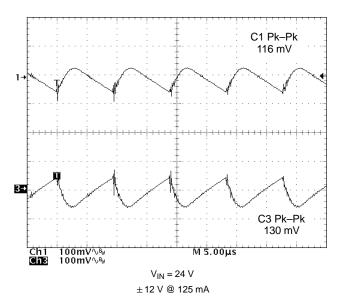


FIGURE 10. Output Voltage Ripple